

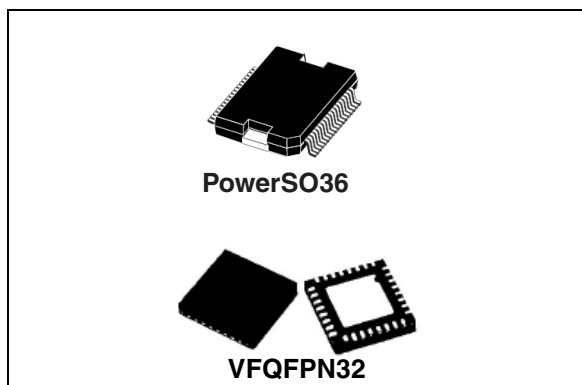
DMOS driver for three-phase brushless DC motor

Features

- Operating supply voltage from 8 to 52 V
- 2.8 A output peak current (1.4 A RMS)
- $R_{DS(on)}$ 0.73 Ω typ. value @ $T_J = 25\text{ }^\circ\text{C}$
- Integrated fast free wheeling diodes
- Operating frequency up to 100 kHz
- Non dissipative overcurrent detection and protection
- Cross conduction protection
- Diagnostic output
- Uncommitted comparator
- Thermal shutdown
- Under voltage lockout

Application

- BLDC motor driving
- Sinusoidal / 6-steps driving
- Field oriented control driving system



Description

The L6230 is a DMOS fully integrated three-phase motor driver with overcurrent protection, optimized for FOC application thanks to the independent current senses.

Realized in BCDmultipower technology, the device combines isolated DMOS Power Transistors with CMOS and bipolar circuits on the same chip.

An uncommitted comparator with open-drain output is available.

Available in PowerSO36 and VFQFPN-32 5x5 packages the L6230 features a non dissipative overcurrent protection on the high side power MOSFETs and thermal shutdown.

Table 1. Device summary

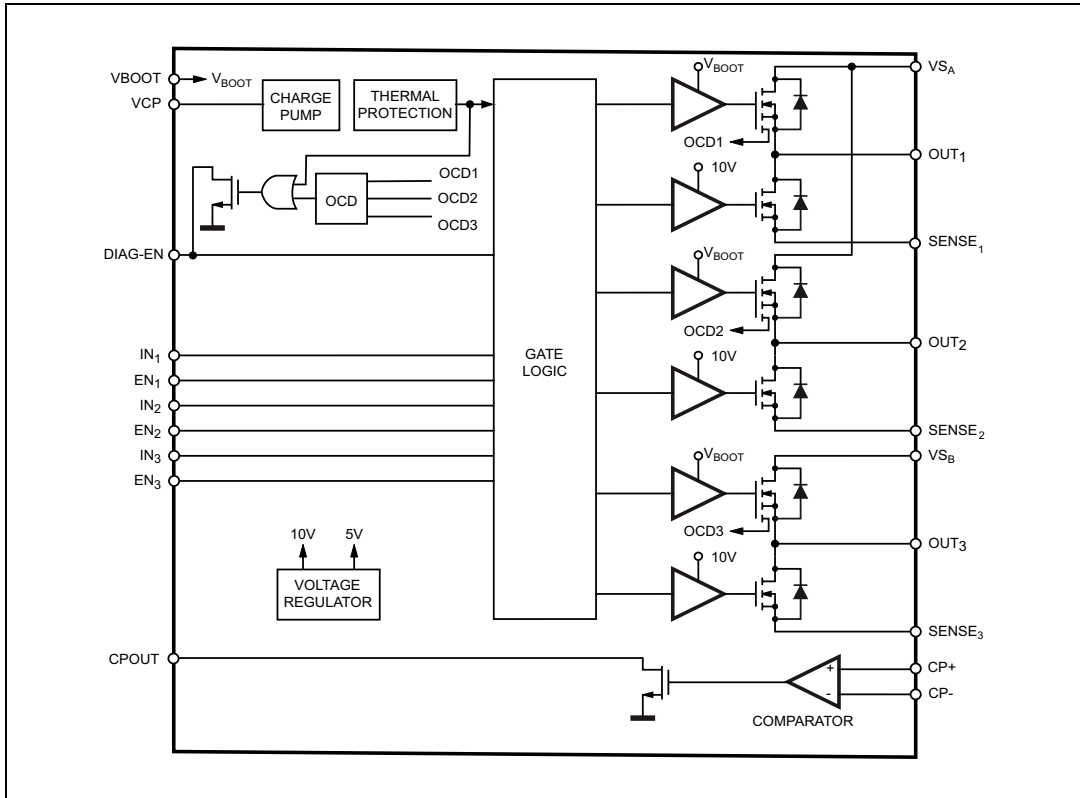
Order codes	Package	Packaging
L6230PD	PowerSO36	Tube
L6230PDTR		Tape and reel
L6230Q	VFQFPN32	Tube
L6230QTR		Tape and reel

Contents

- 1 Block diagram 3**
- 2 Electrical data 4**
 - 2.1 Absolute maximum ratings 4
 - 2.2 Recommended operating conditions 4
 - 2.3 Thermal data 5
- 3 Pin connection 6**
- 4 Electrical characteristics 8**
- 5 Circuit description 11**
 - 5.1 Power stages and charge pump 11
 - 5.2 Logic inputs 12
 - 5.3 Non-dissipative overcurrent detection and protection 13
- 6 Application information 15**
 - 6.1 Field oriented control driving method 15
 - 6.2 Six-step driving method with current control 16
 - 6.3 Six-step driving method with BEMF zero crossing detection 17
 - 6.4 Thermal management 18
- 7 Package mechanical data 19**
- 8 Revision history 23**

1 Block diagram

Figure 1. Block diagram



2 Electrical data

2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Parameter	Value	Unit
V_S	Supply voltage	$V_{SA} = V_{SB} = V_S$	60	V
V_{OD}	Differential voltage between: VSA, OUT1, OUT2, SENSEA and VSB, OUT3, SENSEB	$V_{SA} = V_{SB} = V_S = 60\text{ V};$ $V_{SENSEx} = \text{GND}$	60	V
V_{BOOT}	Bootstrap peak voltage	$V_{SA} = V_{SB} = V_S$	$V_S + 10$	V
V_{IN}, V_{EN}	Logic inputs voltage range		-0.3 to +7	V
V_{CP-}, V_{CP+}	Voltage range at CP- and CP+ pins		-0.3 to +7	V
V_{SENSE}	Voltage range at SENSEx pins		-1 to +4	V
$I_{S(\text{peak})}$	Pulsed supply current (for each VS pin)	$V_{SA} = V_{SB} = V_S;$ $T_{PULSE} < 1\text{ ms}$	3.55	A
I_S	RMS supply current (for each VS pin)	$V_{SA} = V_{SB} = V_S$	1.4	A
T_{stg}, T_{OP}	Storage and operating temperature range		-40 to 150	°C

2.2 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Parameter	Parameter	Min	Max	Unit
V_S	Supply voltage	$V_{SA} = V_{SB} = V_S$	8	52	V
V_{OD}	Differential voltage between VSA, OUT1A, OUT2A, SENSEA and VSB, OUT1B, OUT2B, SENSEB	$V_{SA} = V_{SB} = V_S;$ $V_{SENSE1} = V_{SENSE2} = V_{SENSE3}$		52	V
V_{CP-}, V_{CP+}	Voltage range at CP- and CP+ pins		-0.1	5	V
V_{CPCM}	Common mode voltage at the comparator inputs		0	3	V
V_{SENSE}	Voltage range at pins SENSEx	pulsed $t_W < t_{rr}$	-6	6	V
		DC	-1	1	V
I_{OUT}	RMS output current			1.4	A
T_J	Operating junction temperature		-25	+125	°C
f_{sw}	Switching frequency			100	kHz

2.3 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value		Unit
		PowerSO36	QFN32	
$R_{th(j-amb)1}$	Maximum thermal resistance junction-ambient ⁽¹⁾	36	-	°C/W
$R_{th(j-amb)1}$	Maximum thermal resistance junction-ambient ⁽²⁾	16	-	°C/W
$R_{th(j-amb)2}$	Maximum thermal resistance junction-ambient ⁽³⁾	63	-	°C/W
$R_{th(j-amb)3}$	Maximum thermal resistance junction-ambient ⁽⁴⁾	-	42	°C/W

1. Mounted on a multi-layer FR4 PCB with a dissipating copper surface on the top side of 6 cm² (with a thickness of 35 μm).
2. Mounted on a multi-layer FR4 PCB with a dissipating copper surface on the top side of 6 cm² (with a thickness of 35 μm), 16 via holes and a ground layer.
3. Mounted on a multi-layer FR4 PCB without any heat-sinking surface on the board.
4. Mounted on a double-layer FR4 PCB with a dissipating copper surface of 0.5 cm² on the top side plus 6 cm² ground layer connected through 18 via holes (9 below the IC).

3 Pin connection

Figure 2. Pin connection PowerSO36 (top view)

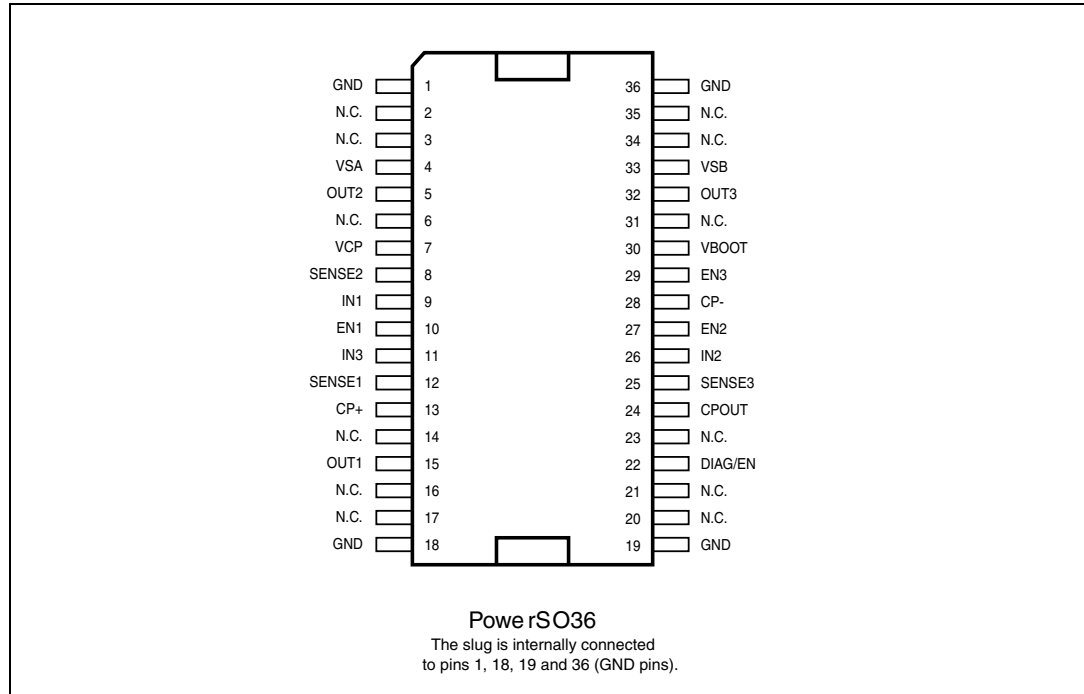
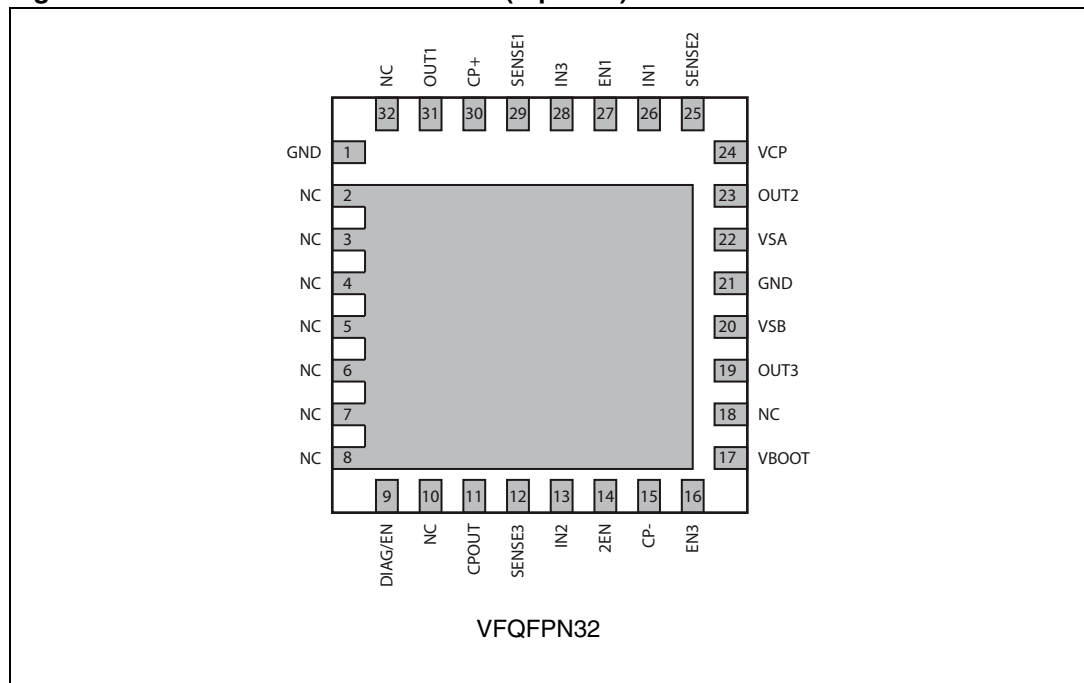


Figure 3. Pin connection VFQFPN32 (top view)



Note: The pins 2 to 8 are connected to die PAD.
The die PAD must be connected to GND pin.

Table 5. Pin description

Pin	Type	Function
VBOOT	Power supply	Bootstrap voltage needed for driving the upper power MOSFETs.
VCP	Output	Charge pump oscillator output.
DIAG-EN	Logic output/input	Double function: chip Enable as input and Overcurrent/Over-temperature indication as output. LOW logic level switches OFF all Power MOSFETs, putting the power stages in high impedance status. An internal open drain transistor pulls to GND the pin when an overcurrent on one of the High Side MOSFETs is detected or during Thermal Protection.
IN1	Logic input	Logic input half bridge 1.
EN1	Logic input	Enable input half bridge 1.
IN2	Logic input	Logic input half bridge 2.
EN2	Logic input	Enable input half bridge 2.
IN3	Logic input	Logic input half bridge 3.
EN3	Logic input	Enable input half bridge 3.
CP-	Analog input	Inverting input of internal comparator.
CP+	Analog input	Non-Inverting input of internal comparator.
CPOUT	Output	Open-drain output of internal comparator.
SENSE3		Half bridge 3 source pin. This pin must be connected to power ground through a sensing power resistor.
OUT3	Power output	Output half bridge 3.
VSB	Power supply	Half bridge 3 power supply voltage. it must be connected to the supply voltage together with pin VSA.
SENSE2		Half bridge 2 source pin. This pin must be connected to power ground through a sensing power resistor.
OUT2	Power output	Output half bridge 2.
SENSE1		Half bridge 1 source pin. This pin must be connected to power ground through a sensing power resistor.
OUT1	Power output	Output half bridge 1.
VSA	Power supply	Half bridge 1 and half bridge 2 power supply voltage. It must be connected to the supply voltage together with pin VSB.
GND	Ground	Ground terminal.

4 Electrical characteristics

($V_S = 48\text{ V}$, $T_A = 25\text{ °C}$, unless otherwise specified)

Table 6. Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$V_{StH(ON)}$	Turn-on threshold		5.8	6.3	6.8	V
$V_{StH(OFF)}$	Turn-off threshold		5	5.5	6	V
I_S	Quiescent supply current	All bridges OFF; $T_J = -25\text{ °C to }125\text{ °C}^{(1)}$		5	10	mA
$T_{j(OFF)}$	Thermal shutdown temperature			165		°C
Output DMOS transistors						
$R_{DS(on)}$	High-side / low-side switch ON resistance	$T_J = 25\text{ °C}$		0.73	0.85	Ω
		$T_J = 125\text{ °C}^{(1)}$		1.18	1.35	Ω
I_{DSS}	Leakage current	DIAG-EN = LOW; OUT = V_S			2	mA
		DIAG-EN = LOW; OUT = GND	-0.3			mA
Source drain diodes						
V_{SD}	Forward ON voltage	$I_{SD} = 1.4\text{ A}$, DIAG-EN = LOW		1.15	1.3	V
t_{rr}	Reverse recovery time	$I_f = 1.4\text{ A}$		300		ns
t_{fr}	Forward recovery time			200		ns
Logic inputs (INx, ENx, DIAG-EN)						
V_{IL}	Low level logic input voltage				0.8	V
V_{IH}	High level logic input voltage		2			V
I_{IL}	Low level logic input current	GND logic input voltage	-10			μA
I_{IH}	High level logic input current	7 V logic input voltage			10	μA
Switching characteristics						
$t_{D(ON)EN}$	Enable to output turn-on delay time ⁽²⁾	$I_{LOAD} = 1.4\text{ A}$, resistive load	500	650	800	ns
$t_{D(OFF)EN}$	Enable to output turn-off delay time ⁽²⁾		500		1000	ns
$t_{D(ON)IN}$	Other logic inputs to OUT turn-ON delay time			1.6		μs
$t_{D(OFF)IN}$	Other logic inputs to OUT turn-OFF delay time			800		ns
t_{RISE}	Output rise time ⁽²⁾		40		250	ns
t_{FALL}	Output fall time ⁽²⁾		40		250	ns
t_{DT}	Dead time		0.5	1		μs
f_{CP}	Charge pump frequency		$T_J = -25\text{ °C to }125\text{ °C}^{(1)}$		0.6	1

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Comparator						
V_{OFFSET}	Offset voltage	$V_{\text{CP-}} = 0.5 \text{ V}$	-14		+14	mV
t_{prop}	Propagation delay	(3)		500		ns
I_{BIAS}	Inputs bias current				10	μA
R_{CPOUT}	Open drain ON resistance			40	60	Ω
Over current detection and protection						
I_{SOVER}	Supply overcurrent protection threshold	$T_{\text{J}} = -25 \text{ to } 125 \text{ }^\circ\text{C}$ (1)	2	2.8	3.55	A
R_{DIAG}	Open drain ON resistance	$I_{\text{DIAG}} = 4 \text{ mA}$		40	60	Ω
$t_{\text{OCD(ON)}}$	OCD turn-ON delay time (4)	$I_{\text{DIAG}} = 4 \text{ mA}; C_{\text{DIAG}} < 100 \text{ pF}$		200		ns
$t_{\text{OCD(OFF)}}$	OCD turn-OFF delay time (4)	$I_{\text{DIAG}} = 4 \text{ mA}; C_{\text{DIAG}} < 100 \text{ pF}$		100		ns

1. Tested at 25 °C in a restricted range and guaranteed by characterization
2. See [Figure 4](#).
3. Measured applying a voltage of 1 V to pin CP+ and a voltage drop from 2 V to 0 V to pin CP-.
4. See [Figure 5](#).

Figure 4. Switching characteristic definition

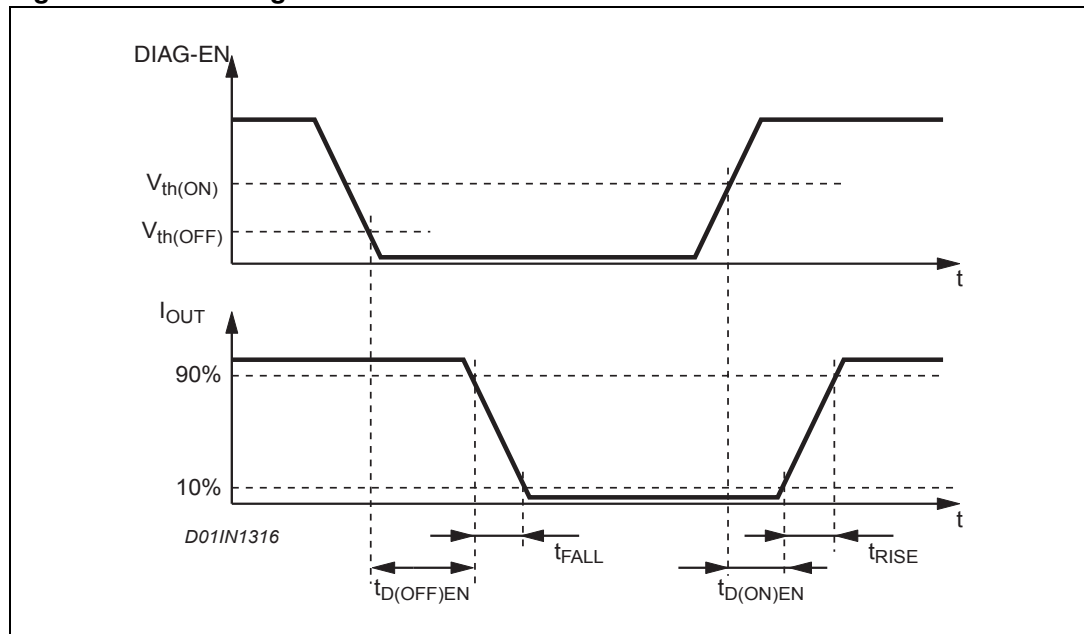
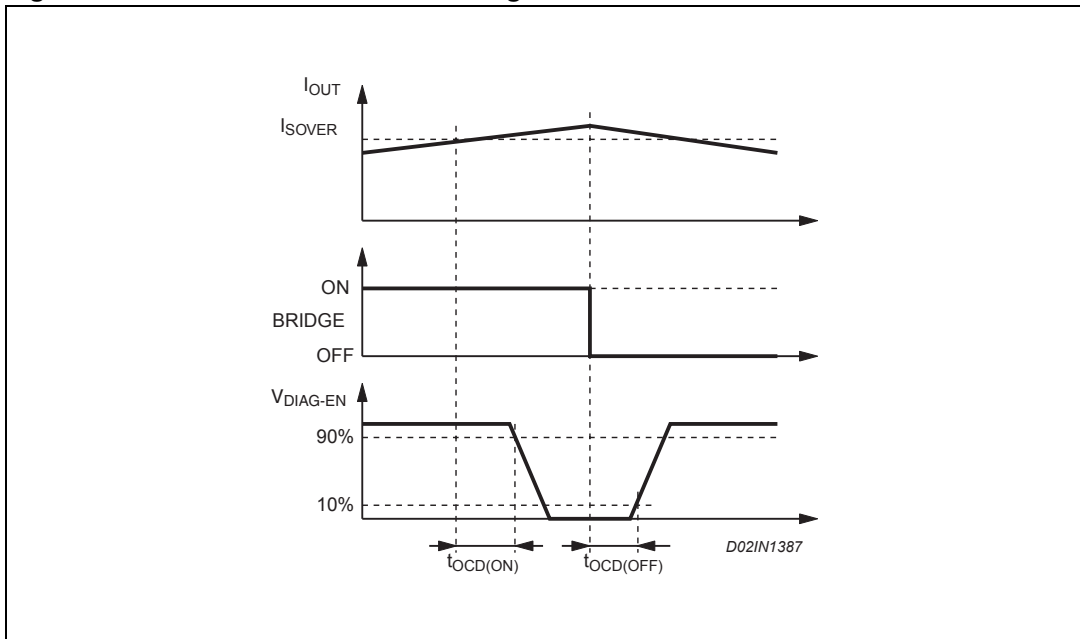


Figure 5. Overcurrent detection timing definition



5 Circuit description

5.1 Power stages and charge pump

The L6230 integrates a three-phase bridge, which consists of 6 power MOSFETs connected as shown on the block diagram (see [Figure 1](#)), each power MOS has an $R_{DS(ON)} = 0.73 \Omega$ (typical value @ 25 °C) with intrinsic fast freewheeling diode. Cross conduction protection is implemented by using a dead time ($t_{DT} = 1 \mu s$ typical value) set by internal timing circuit between the turn off and turn on of two power MOSFETs in one leg of a bridge.

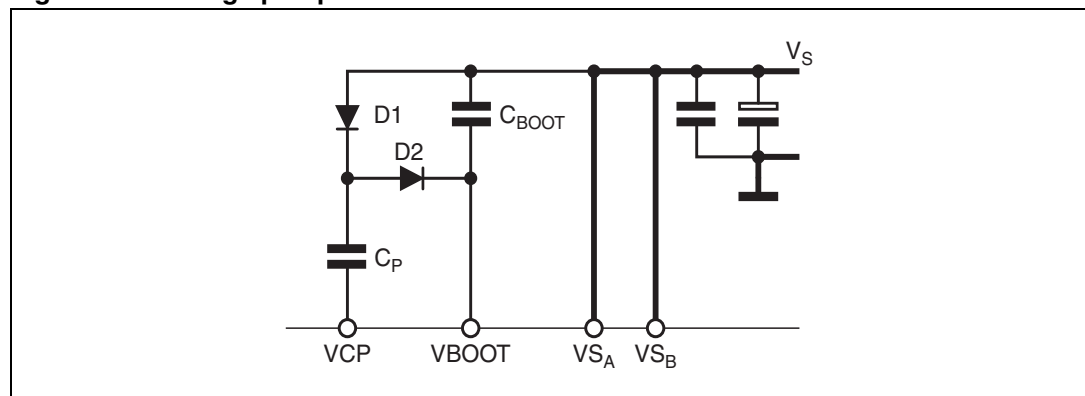
Pins VS_A and VS_B must be connected together to the supply voltage (V_S).

Using N-channel power MOS for the upper transistors in the bridge requires a gate drive voltage above the power supply voltage. The bootstrapped supply (V_{BOOT}) is obtained through an internal oscillator and few external components to realize a charge pump circuit as shown in [Figure 6](#). The oscillator output (pin VCP) is a square wave at 600 kHz (typically) with 10 V amplitude. Recommended values/part numbers for the charge pump circuit are shown in [Table 7](#).

Table 7. Charge pump external component values

Component	Value
C_{BOOT}	220 nF
C_P	10 nF
D1	1N4148
D2	1N4148

Figure 6. Charge pump circuit



5.2 Logic inputs

Pins INx and ENx are TTL/CMOS and microcontroller compatible logic inputs. The internal structure is shown in [Figure 7](#). Typical value for turn-on and turn-off thresholds are respectively $V_{th(ON)} = 1.8\text{ V}$ and $V_{th(OFF)} = 1.3\text{ V}$.

Pin DIAG-EN has identical input structure with the exception that the drain of the Overcurrent and thermal protection MOSFET is also connected to this pin. Due to this connection some care needs to be taken in driving this pin. The EN input may be driven in one of two configurations as shown in [Figure 8](#) or [Figure 9](#). If driven by an open drain (collector) structure, a pull-up resistor R_{EN} and a capacitor C_{EN} are connected as shown in [Figure 8](#). If the driver is a standard Push-Pull structure the resistor R_{EN} and the capacitor C_{EN} are connected as shown in [Figure 9](#). The resistor R_{EN} should be chosen in the range from 2.2 kΩ to 180 kΩ. Recommended values for R_{EN} and C_{EN} are respectively 10 kΩ and 5.6 nF. More information on selecting the values is found in the overcurrent protection section.

Figure 7. Logic inputs internal structure

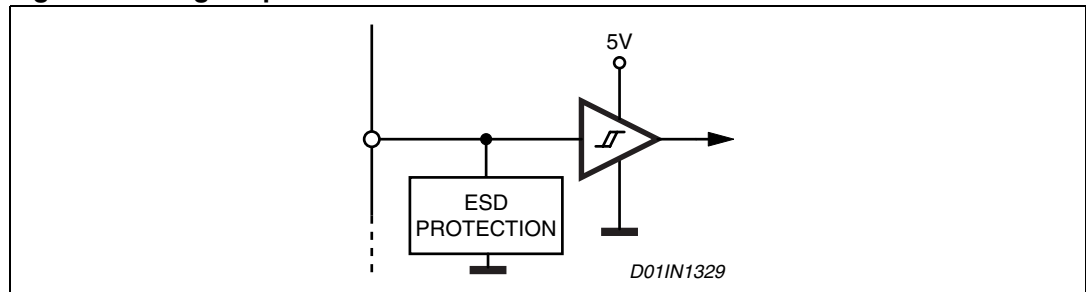


Figure 8. Pin DIAG-EN open collector driving

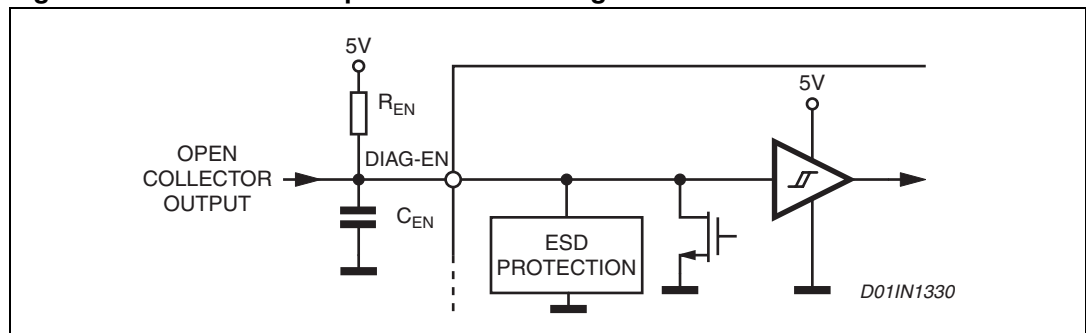
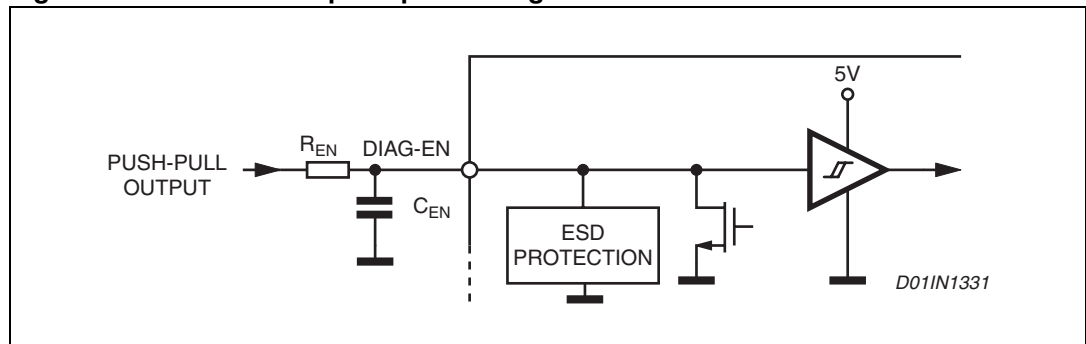


Figure 9. Pin DIAG-EN push-pull driving



5.3 Non-dissipative overcurrent detection and protection

The L6230 integrates an overcurrent detection circuit (OCD) for full protection. This circuit provides output-to-output and output-to-ground short circuit protection as well. With this internal over current detection, the external current sense resistor normally used and its associated power dissipation are eliminated. *Figure 10* shows a simplified schematic for the overcurrent detection circuit.

To implement the over current detection, a sensing element that delivers a small but precise fraction of the output current is implemented with each high side power MOS. Since this current is a small fraction of the output current there is very little additional power dissipation. This current is compared with an internal reference current I_{REF} . When the output current reaches the detection threshold (typically $I_{SOVER} = 2.8$ A) the OCD comparator signals a fault condition. When a fault condition is detected, an internal open drain MOS with a pull down capability of 4 mA connected to pin DIAG is turned on.

The pin DIAG-EN can be used to signal the fault condition to a μ C and to shut down the three-phase bridge simply by connecting the pin to an external R-C (see R_{EN} , C_{EN}).

Figure 10. Overcurrent protection simplified schematic

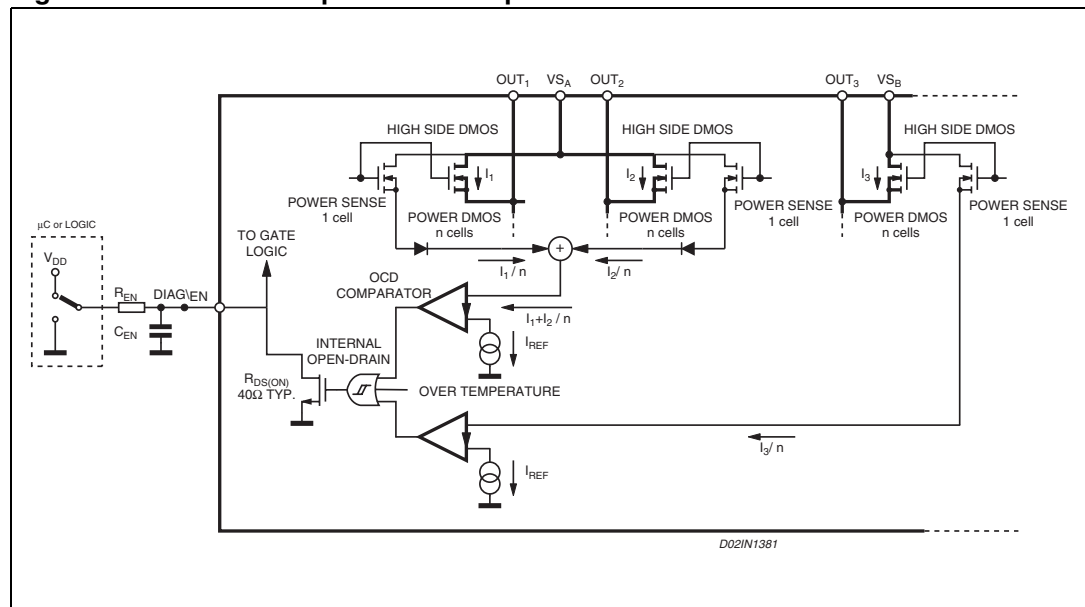


Figure 11 shows the overcurrent detection operation. The disable time $t_{DISABLE}$ before recovering normal operation can be easily programmed by means of the accurate thresholds of the logic inputs. It is affected whether by C_{EN} and R_{EN} values and its magnitude is reported in *Figure 12*. The delay time t_{DELAY} before turning off the bridge when an overcurrent has been detected depends only by C_{EN} value. Its magnitude is reported in *Figure 13*

C_{EN} is also used for providing immunity to pin DIAG-EN against fast transient noises. Therefore the value of C_{EN} should be chosen as big as possible according to the maximum tolerable delay time and the R_{EN} value should be chosen according to the desired disable time.

The resistor R_{EN} should be chosen in the range from 2.2 k Ω to 180 k Ω . Recommended values for R_{EN} and C_{EN} are respectively 100 k Ω and 5.6 nF that allow obtaining 200 μ s disable time.

Figure 11. Overcurrent protection waveforms

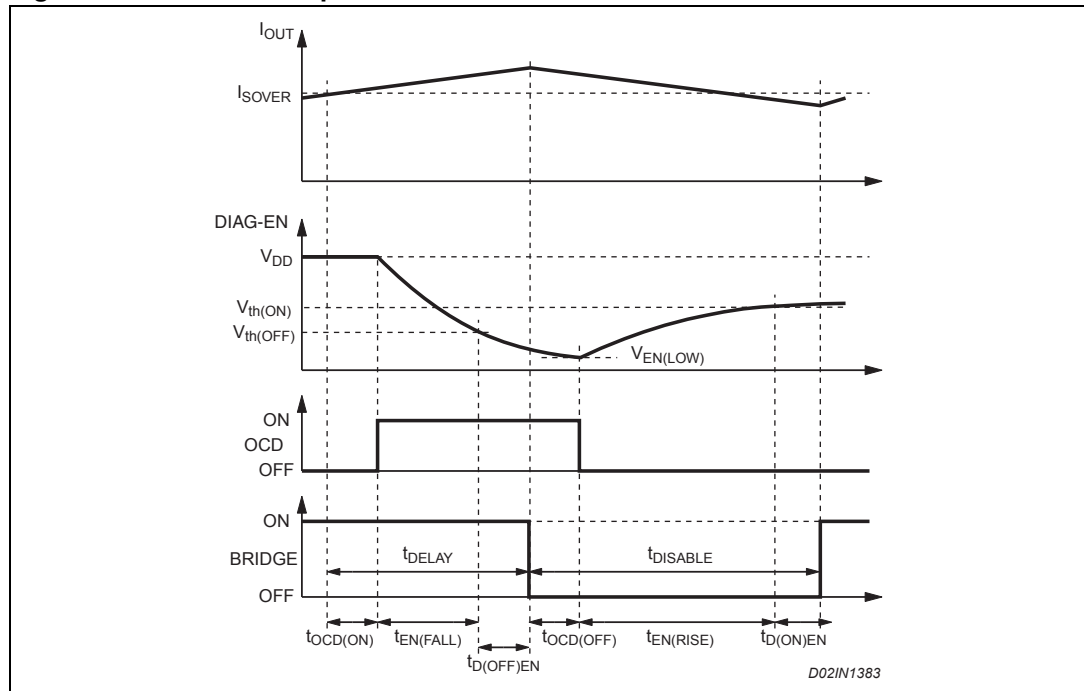


Figure 12. $t_{DISABLE}$ versus C_{EN} and R_{EN}

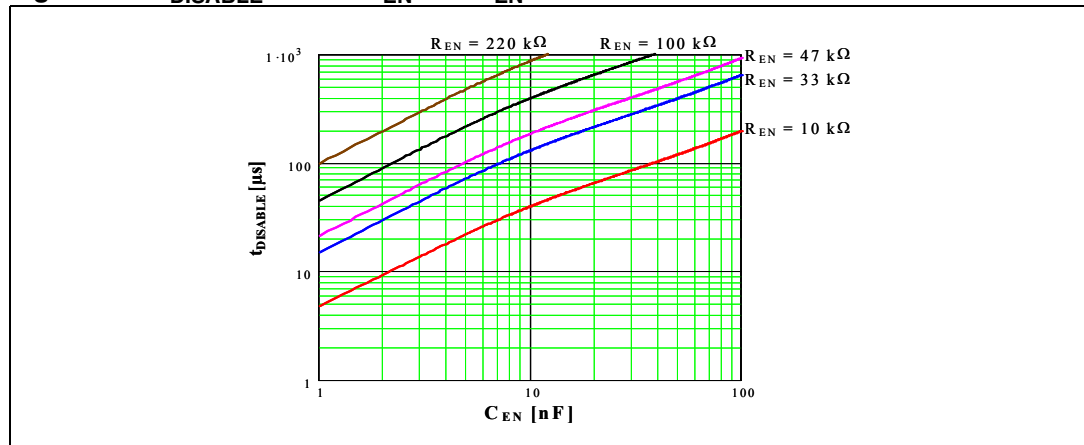
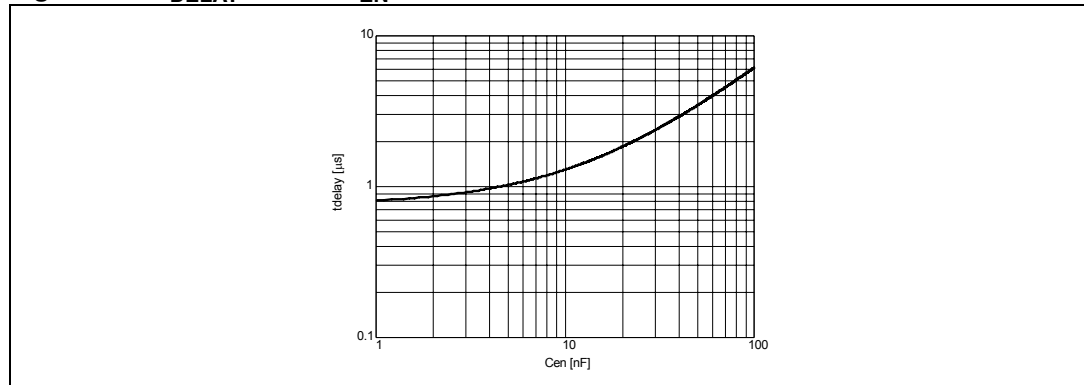


Figure 13. t_{DELAY} versus C_{EN}



6 Application information

Some typical applications using L6230 are shown in this paragraph. A high quality ceramic capacitor (C_2) in the range of 100 nF to 200 nF should be placed between the power pins VS_A and VS_B and ground near the L6230 to improve the high frequency filtering on the power supply and reduce high frequency transients generated by the switching. The capacitor (C_{EN}) connected from the DIAG-EN input to ground sets the shut down time when an over current is detected (see overcurrent protection). The current sensing inputs ($SENSE_X$) should be connected to the sensing resistors R_{SENSE} with a trace length as short as possible in the layout. The sense resistors should be non-inductive resistors to minimize the di/dt transients across the resistors. To increase noise immunity, unused logic pins are best connected to 5 V (high logic level) or GND (low logic level) (see pin description). It is recommended to keep power ground and signal ground separated on PCB.

Table 8. Component values for typical application

Component	Value
C_1	100 μ F
C_2	100 nF
C_{BOOT}	220 nF
C_{EN}	5.6 nF
C_P	10 nF
D_1	1N4148
D_2	1N4148
R_{EN}	100 k Ω

The examples reported describe some typical application to drive a 3-phase BLDC motor using L6230 device.

In the first example is shown a field oriented control (FOC) system, with this method it is possible to provide smooth and precise motor control of BLDC motors.

A six-step driving method with current control is reported in the second example, the inputs sequence is generated by external controller and the L6230 comparator is used to obtain the information for the peak current control.

Finally, the third example shows how to implement a sensorless motor control system, the information on rotor position is achieved by BEMF zero-crossing detection.

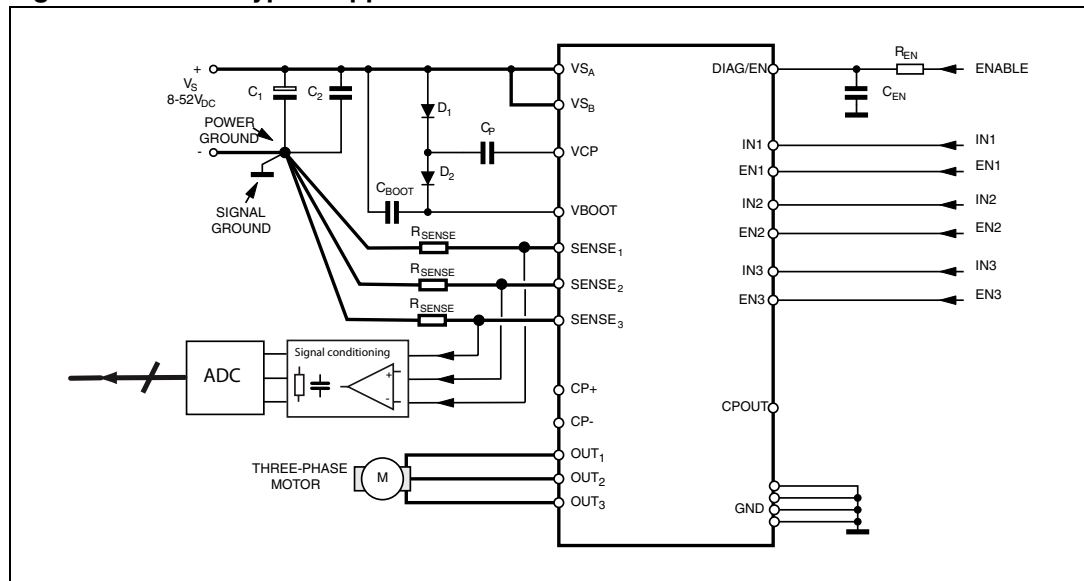
6.1 Field oriented control driving method

In this configuration (see [Figure 14](#)) three sensing resistors are required, one for each channel. The sensing signals coming from the output power stage are conditioned by external operational amplifiers which provide the proper feedback signals to the AtoD converter and the system controller. According to the feedback signals the six input lines are generated by the controller.

Note that some filtering and level shifting RC networks should be added between the sense resistor and the correspondent op-amp input.

The uncommitted internal comparator with open-drain output is available.

Figure 14. F.O.C. typical application



6.2 Six-step driving method with current control

In this configuration only one sense resistor are needed, the three OUT pins are connected together to R_{SENSE} (see [Figure 15](#)).

The non-inverting input comparator CP+ monitors the voltage drop across the external sense resistor connected between the source of the three lower power MOS transistors and ground.

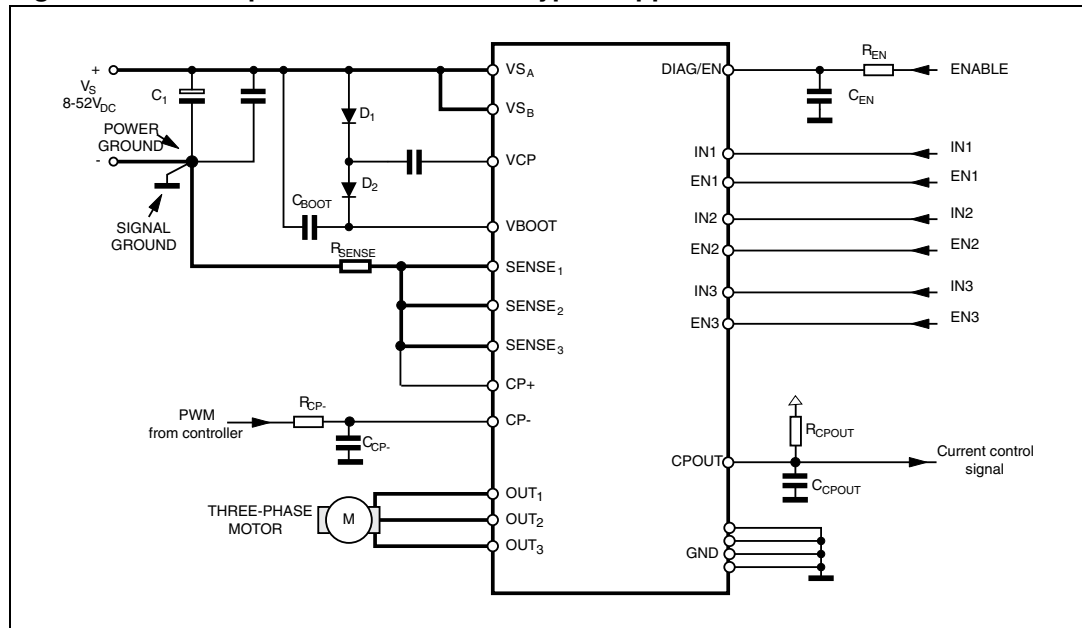
As the current in the motor increases the voltage across the R_{SENSE} increases proportionally. When the voltage drop across the sense resistor becomes greater than the reference voltage applied at inverting input CP- the comparator open-drain output is switched on pulling down the CPOUT pin.

This signal could be managed by controller to generate the proper input sequence for six-step driving method with current control and select what current decay method to implement.

When the sense voltage decrease below the CP- voltage, the open-drain is switched off and the voltage at CPOUT pin start to increase charging the capacitor C3.

The reference voltage at pin CP- will be set according to sense resistor value and the desired regulated current ($V_{CP-} \cong R_{SENSE} \times I_{TARGET}$). A very simple way to obtain variable voltage is to low-pass filter a PWM output of a controller.

Figure 15. Six-step with current control typical application



6.3 Six-step driving method with BEMF zero crossing detection

The BEMF zero crossing information can be used to evaluate the rotor position; in this way no Hall effect sensors or encoder are needed.

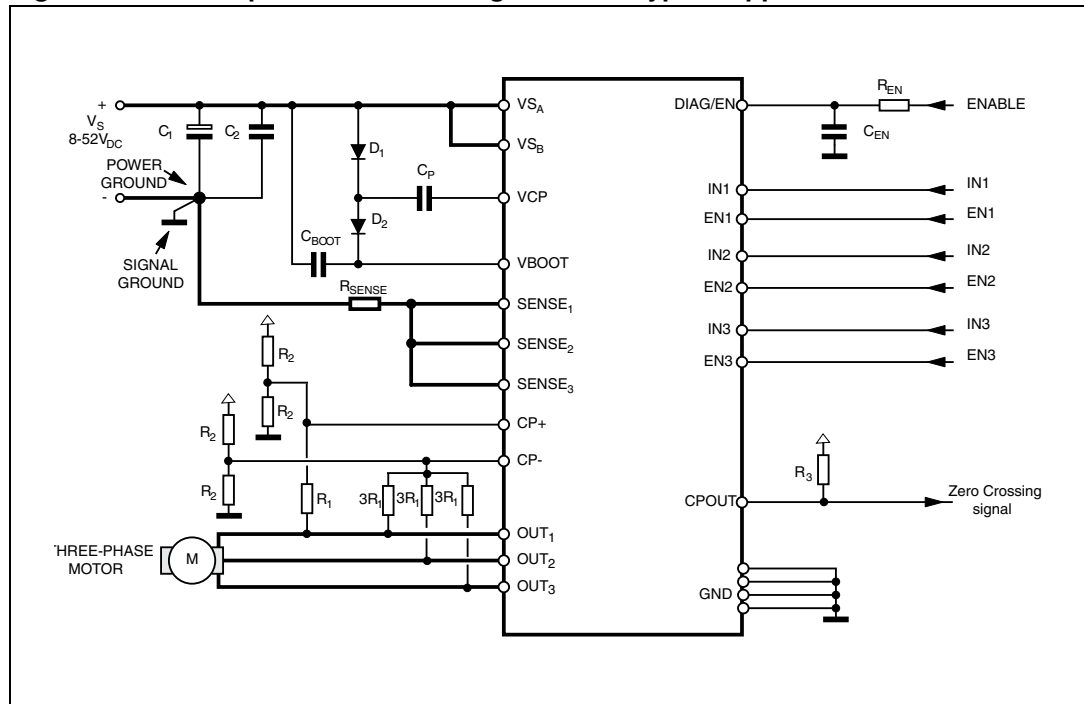
In six-step driving mode one of the three phases is left in high impedance state.

Comparing the voltage of this phase with the center-tap voltage we can detect the BEMF zero-crossing.

In shown example (see [Figure 16](#)), the OUT1 phase voltage is monitored by the CP+; the center-tap voltage is obtained as combination of three phase voltages and monitored by the CP- pin. Only when the OUT1 is in high impedance, the CPOUT will perform a commutation each time a BEMF zero crossing is detected.

In this configuration one sense resistor is needed, the three OUT pins are connected together to R_{SENSE} .

Figure 16. Six-step with zero crossing detection typical application



6.4 Thermal management

In most applications the power dissipation in the IC is the main factor that sets the maximum current that can be delivered by the device in a safe operating condition. Therefore, it has to be taken into account very carefully. Besides the available space on the PCB, the right package should be chosen considering the power dissipation. Heat sinking can be achieved using copper on the PCB with proper area and thickness.

For instance, using a VFQFPN32L 5 x 5 package the typical $R_{th(JA)}$ is about 42 °C/W when mounted on a double-layer FR4 PCB with a dissipating copper area of 0.5 cm² on the top side plus 6 cm² ground layer connected through 18 via holes (9 below the IC).

Otherwise, using a PowerSO package with copper slug soldered on a 1.5 mm copper thickness FR4 board with 6cm² dissipating footprint (copper thickness of 35 μm), the $R_{th(jA)}$ is about 35°C/W.

Using a multi-layer board with vias to a ground plane, thermal impedance can be reduced down to 15°C/W.

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 9. VFQFPN 5 x 5 x 1.0, 32 lead, pitch 0.50

Dim.	Databook (mm)		
	Min	Typ	Max
A	0.80	0.85	0.95
b	0.18	0.25	0.30
b1	0.165	0.175	0.185
D	4.85	5.00	5.15
D2	3.00	3.10	3.20
D3	1.10	1.20	1.30
E	4.85	5.00	5.15
E2	4.20	4.30	4.40
E3	0.60	0.70	0.80
e		0.50	
L	0.30	0.40	0.50
ddd			0.08

Note: VFQFPN stands for thermally enhanced very thin profile fine pitch quad flat package no lead. Very thin profile: $0.80 < A < 1.00$ mm.

Details of terminal 1 are optional but must be located on the top surface of the package by using either a mold or marked features.

Figure 17. Package dimensions

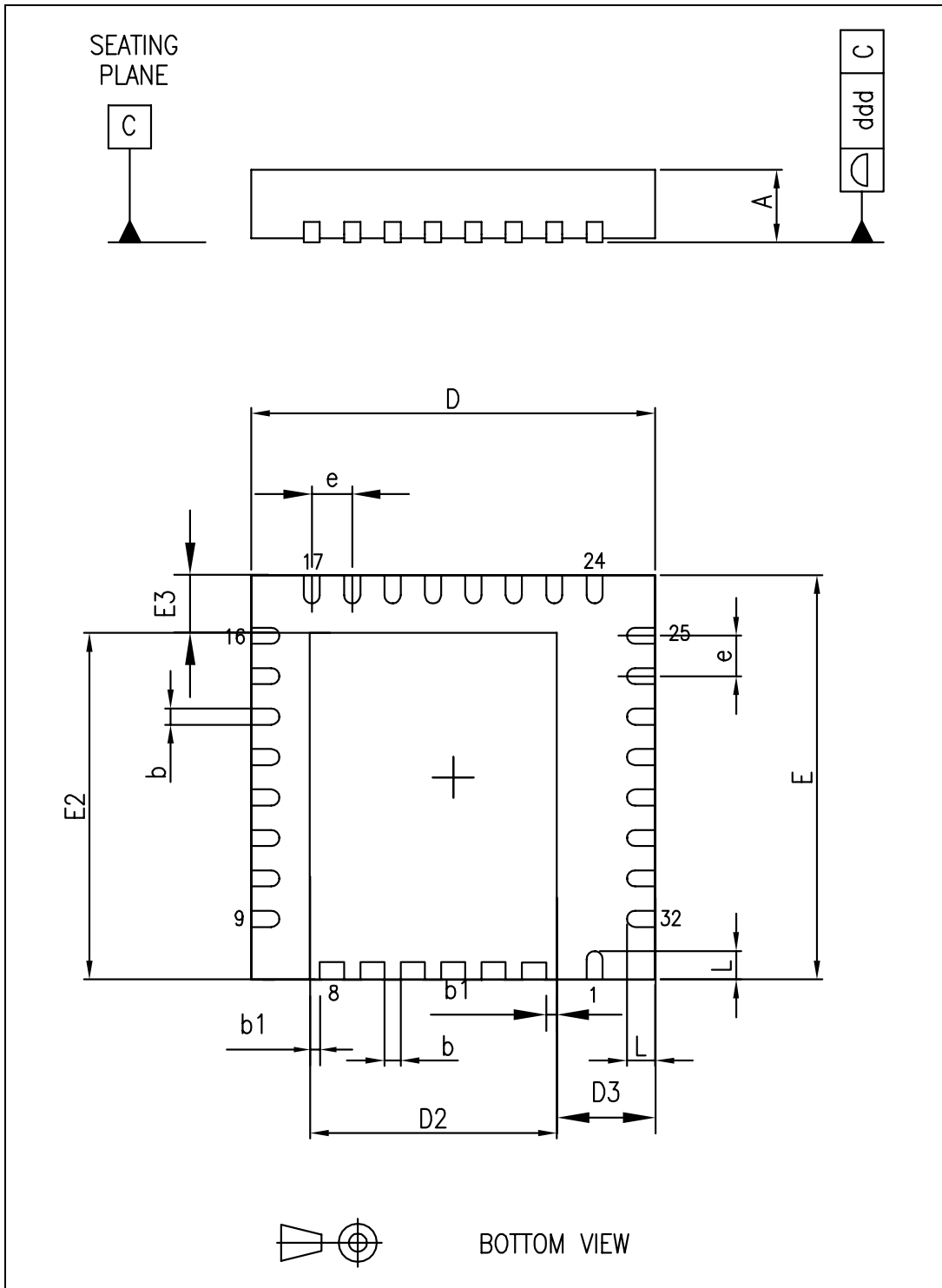
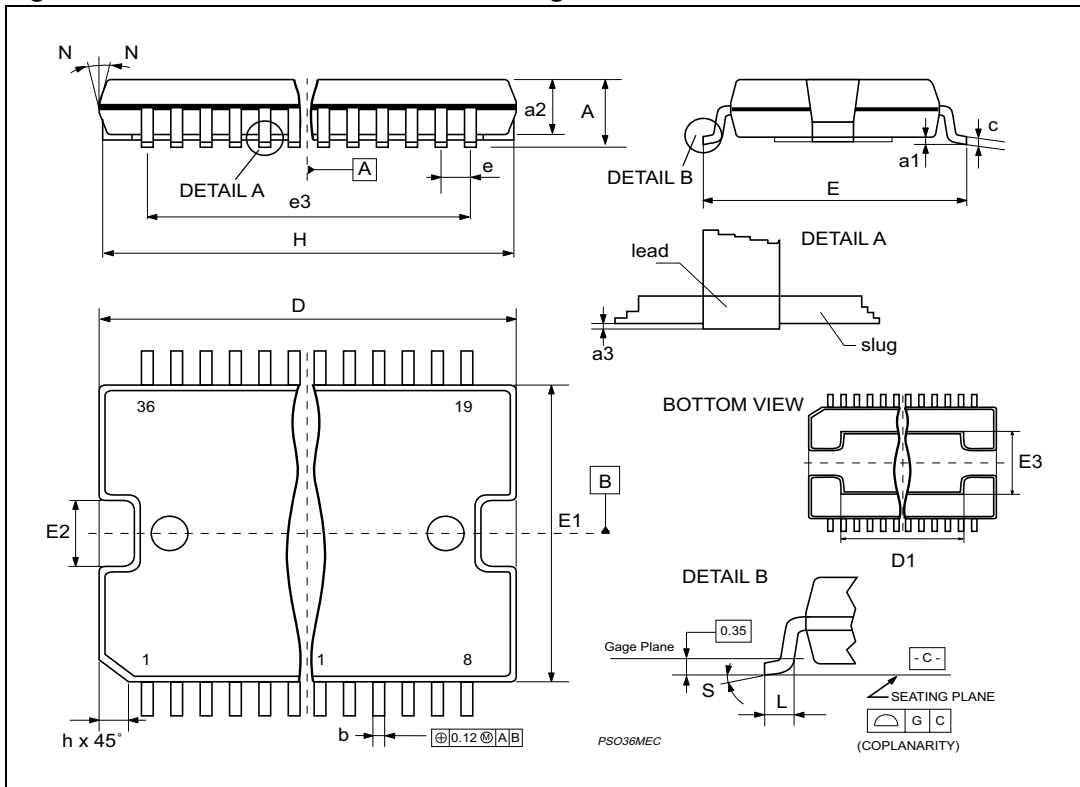


Table 10. PowerSO36 mechanical data

	Min.	Typ.	Max.
A			3.6
a1	0.1		0.3
a2			3.3
a3	0		0.1
b	0.22		0.38
c	0.23		0.32
D (1)	15.8		16
D1	9.4		9.8
E	13.9		14.5
e		0.65	
e3		11.05	
E1 (1)	10.9		11.1
E2			2.9
E3	5.8		6.2
E4	2.9		3.2
G	0		0.1
H	15.5		15.9
h			1.1
L	0.8		1.1
N	10°(max.)		
S	8 °(max.)		

Figure 18. PowerSO36 mechanical drawings



8 Revision history

Table 11. Document revision history

Date	Revision	Changes
14-Oct-2010	1	First release
07-Jun-2011	2	Updated maturity status from preliminary data to final datasheet.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2011 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com